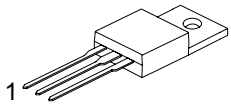
YAREN TECHNOLOGY

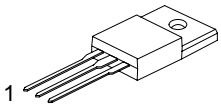
7N60

Power MOSFET

6.5Amps, 600 Volts
N-CHANNEL MOSFET



TO-220



TO-220F

*Pb-free plating product number:7N60

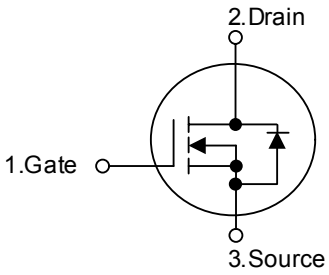
■ DESCRIPTION

The YR 7N60 is a high voltage MOSFET and is designed to have better characteristics, such as fast switching time, low gate charge, low on-state resistance and have a high rugged avalanche characteristics. This power MOSFET is usually used at high speed switching applications in switching power supplies and adaptors.

■ FEATURES

* $R_{DS(ON)}$ = 1.2 Ω@V_{GS} = 10 V
* Low gate and reverse transfer Capacitance (C: 16 pF typical)
* Fast switching capability
* Avalanche energy tested
* Improved dv/dt capability, high ruggedness

■ SYMBOL



■ ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	600	V
Gate-Source Voltage		V_{GSS}	±20	V
Avalanche Current (Note 1)		I_{AR}	6.5	A
Continuous Drain Current	T_C = 25°C	I_D	6.5	A
	T_C = 100°C		4.0	A
Pulsed Drain Current (Note 1)		I_{DM}	29.6	A
Avalanche Energy, Single Pulsed (Note 2)		E_{AS}	580	mJ
Avalanche Energy, Repetitive Limited by $T_{J(MAX)}$		E_{AR}	14.2	mJ
Peak Diode Recovery dv/dt (Note 3)		dv/dt	4.5	V/ns
Power Dissipation (T_C = 25℃)		P_D	142	W
Derate above 25℃			1.14	W/℃
Junction Temperature		T_J	+150	℃
Operating and Storage Temperature		T_{STG}	-55 ~ +150	℃

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Junction-to-Ambient	θ_{JA}			62.5	°C/W
Junction-to-Case	θ_{JC}			0.88	°C/W
Case-to-Sink	θ_{CS}		0.5		°C/W

■ ELECTRICAL CHARACTERISTICS (T_C =25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	600			V
Drain-Source Leakage Current	I_{DSS}	V_{DS} = 600V, V_{GS} = 0V			10	μA
		V_{DS} = 480V, T_C = 125°C			100	μA
Gate-Body Leakage Current, Forward	I_{GSSF}	V_{GS} = 20V, V_{DS} = 0V			100	nA
Gate-Body Leakage Current, Reverse	I_{GSSR}	V_{GS} = -20V, V_{DS} = 0V			-100	nA
Breakdown Voltage Temperature Coefficient	$\triangle BV_{DSS}/\triangle T_J$	I_D = 250μA, Referenced to 25°C		0.67		V/℃
On Characteristics						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0		4.0	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 3.25A		1.0	1.2	Ω
Forward Transconductance	g_{FS}	V_{DS} = 50V, I_D = 3.25A (Note 4)		6.4		S
Dynamic Characteristics						
Input Capacitance	C_{ISS}	V_{DS}=25V, V_{GS}=0V, f=1.0 MHz			1400	pF
Output Capacitance	C_{OSS}				180	pF
Reverse Transfer Capacitance	C_{RSS}				21	pF
Switching Characteristics						
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} =300V, I_D =6.5A, R_G =25Ω (Note 4, 5)			70	ns
Turn-On Rise Time	t_R				170	ns
Turn-Off Delay Time	$t_{d(OFF)}$				140	ns
Turn-Off Fall Time	t_F				130	ns
Total Gate Charge	Q_G	V_{DS}=480V, I_D=6.5A, V_{GS}=10 V (Note 4, 5)		29	38	nC
Gate-Source Charge	Q_{GS}			7		nC
Gate-Drain Charge	Q_{GD}			14.5		nC

■ ELECTRICAL CHARACTERISTICS(Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Drain-Source Diode Characteristics and Maximum Ratings						
Drain-Source Diode Forward Voltage	V_{SD}	V_{GS} = 0V, I_S = 6.5 A			1.4	V
Maximum Continuous Drain-Source Diode Forward Current	I_S				7.0	A
Maximum Pulsed Drain-Source Diode Forward Current	I_{SM}				29.6	A
Reverse Recovery Time	t_{RR}	V_{GS} = 0V, I_S = 6.5 A,		320		ns
Reverse Recovery Charge	Q_{RR}	d_{IF} / dt = 100A/μs (Note 4)		2.4		μC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 19.5mH, I_{AS} = 6.5A, V_{DD} = 50V, R_G = 25 Ω, Starting T_J = 25°C
3. I_{SD} ≤ 6.5A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

■ TEST CIRCUITS AND WAVEFORMS

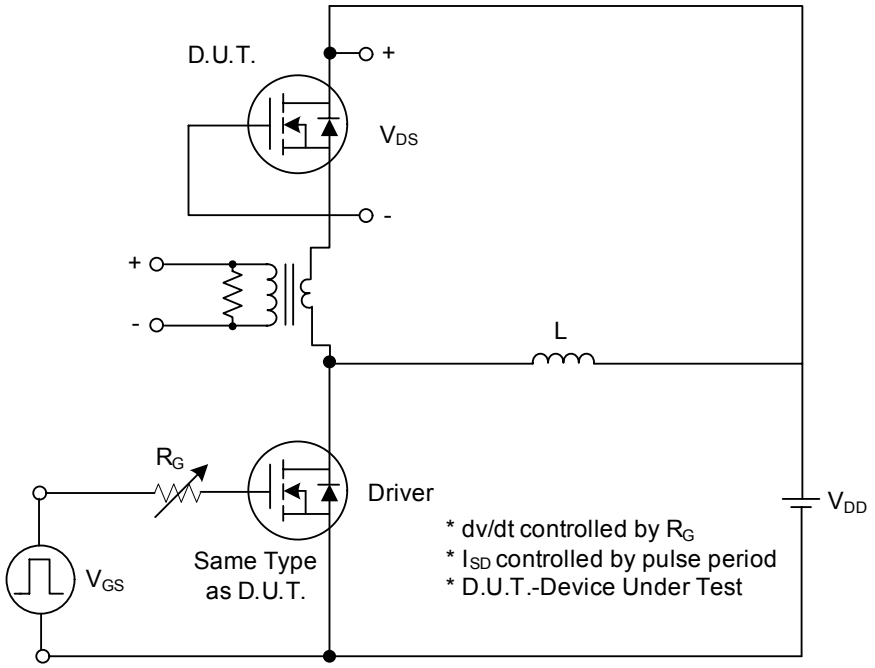


Fig. 1A Peak Diode Recovery dv/dt Test Circuit

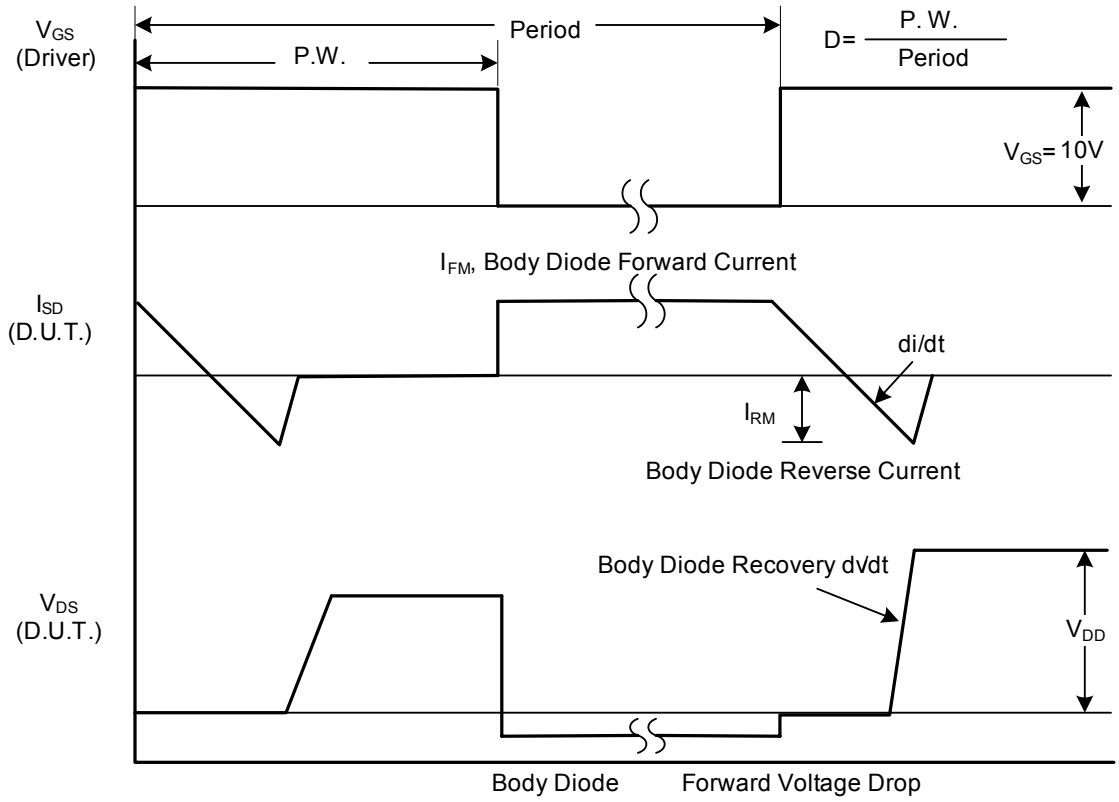


Fig. 1B Peak Diode Recovery dv/dt Waveforms

■ TEST CIRCUITS AND WAVEFORMS (Cont.)

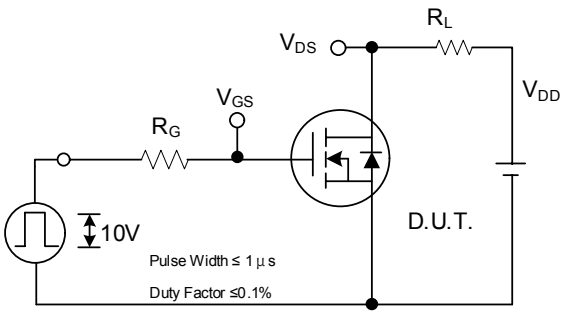


Fig. 2A Switching Test Circuit

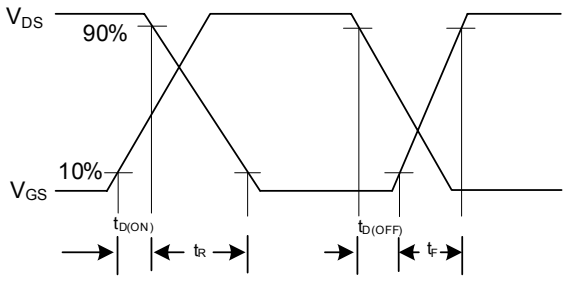


Fig. 2B Switching Waveforms

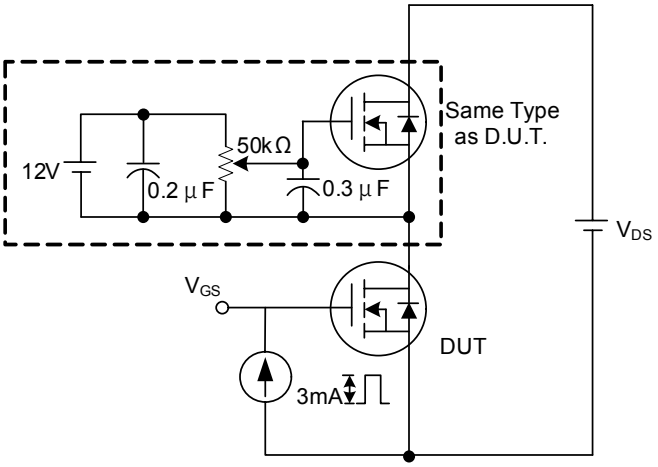


Fig. 3A Gate Charge Test Circuit

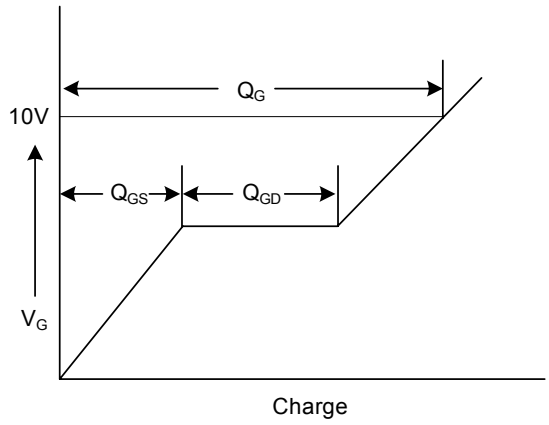


Fig. 3B Gate Charge Waveform

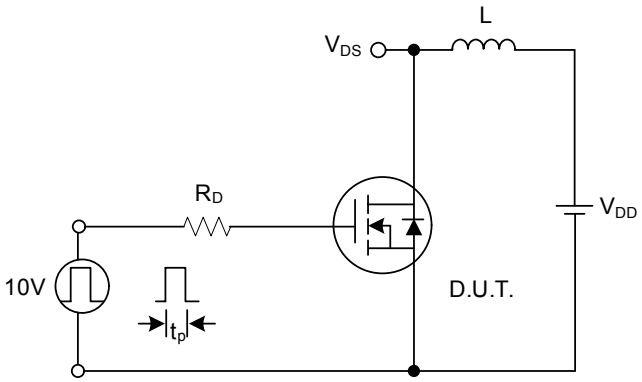


Fig. 4A Unclamped Inductive Switching Test Circuit

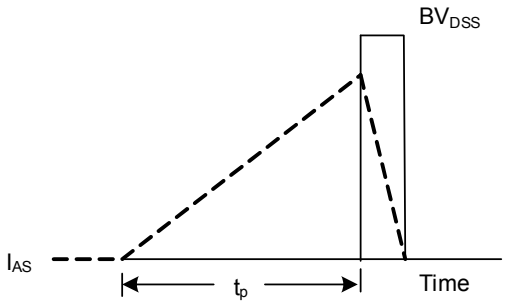


Fig. 4B Unclamped Inductive Switching Waveforms