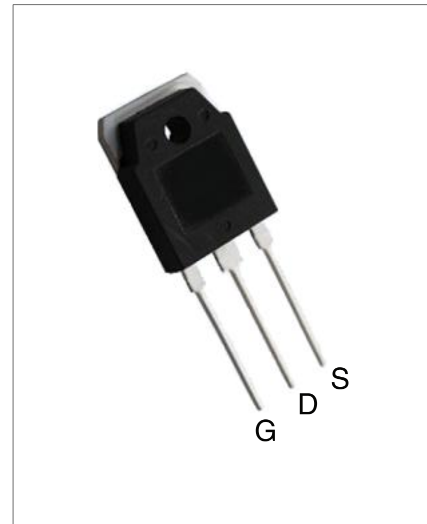
40N25

Power MOSFET

40Amps, 250 Volts
N-CHANNEL MOSFET



*Pb-free plating product number:40N25

■ DESCRIPTION

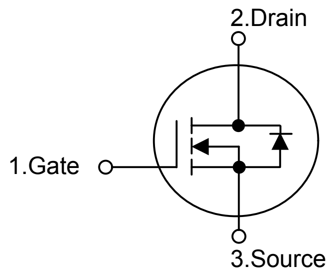
The YR40N25 are N-Channel enhancement mode power field effect transistors (MOSFET) which are produced using YR's proprietary, planar stripe, DMOS technology.

These devices are suited for high efficiency switch mode power supply. To minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode the advanced technology has been especially tailored.

■ FEATURES

* $R_{DS(ON)}$ = 0.10Ω @V_{GS} = 10 V
* Ultra low gate charge (typical 80 nC)
* Low reverse transfer capacitance (C_{RSS} = typical 45 pF)
* Fast switching capability
* Avalanche energy specified
* Improved dv/dt capability, high ruggedness

■ SYMBOL



■ ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, unless otherwise specified)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	250	V
V_{GS}	Gate-source voltage	±16	V
I_D (1)	Drain current (continuous) at T_C= 25°C	36	A
I_D (1)	Drain current (continuous) at T_C= 100°C	23	A
I_{DM} (2)	Drain current (pulsed)	144	A
P_{TOT} (1)	Total dissipation at T_C= 25°C	278	W
dv/dt (3)	Peak diode recovery voltage slope	4	V/ns
T_{stg}	Storage temperature	-55 to 150	°C
T_j	Max. operating junction temperature	150	°C
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj Max)	40	A
E_{AS}	Single pulse avalanche energy (starting Tj=25°C, Id=Iar, Vdd=50V)	320	mJ
E_{AR}	Repetitive avalanche	25	mJ

1. Rated according to the Rthj-case
2. Pulse width limited by safe operating area
3. $I_{SD} \leq$ 40A, di/dt $\leq$ 400A/μs, V_{DD} = 80% $V_{(BR)DSS}$

■ ELECTRICAL CHARACTERISTICS (T_C =25°C, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	80% BV_{Dss}			10	μA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±16V			±100	nA
BV_{DSS}	Drain-to-source breakdown voltage	I_D = 1mA, V_{GS} = 0V	250			V
$V_{GS(th)}$	Gate threshold voltage	V_{DS} =V_{GS}, I_D = 1mA	2		4.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 12V, I_D = 20A		0.084	0.1	Ω

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 0V, f=1MHz, V_{GS}=12V		9100 650 45		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-to-source charge Gate-to-drain (“Miller”) charge	V_{DD} = 200V, I_D = 40A, V_{GS}=12V		202 34 58	280 47 80	nC nC nC
R_G	Gate input resistance	f=1MHz Gate DC Bias=0 Test signal level=20mV open drain		1.4	3	Ω

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off-delay time Fall time	V_{DD} = 125V, I_D =40 A, R_G = 4.7Ω, V_{GS} = 12V		33 80 123 145		ns ns ns ns

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)				36 144	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 40A, V_{GS} = 0			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 40A, di/dt = 100A/μs V_{DD}= 50V, Tj = 150°C		484 8.4 35		ns μC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300μs, duty cycle 1.5%

Figure 1. Safe operating area

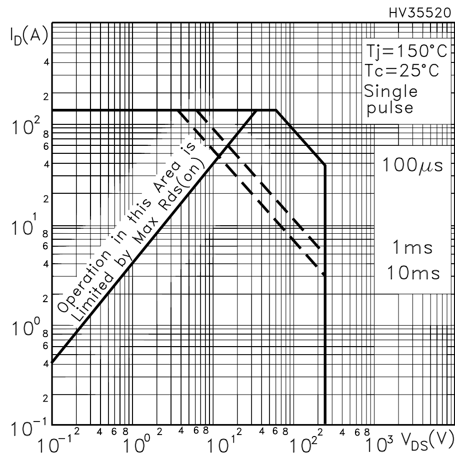


Figure 2. Thermal impedance

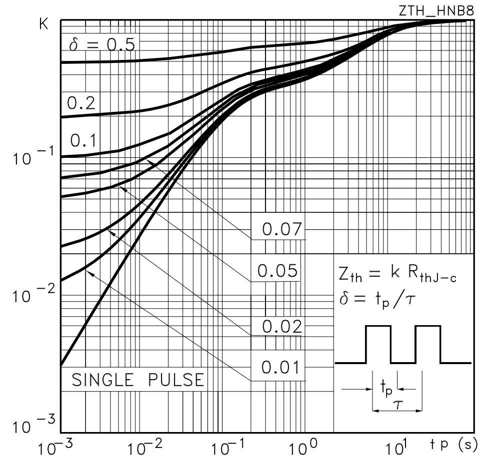


Figure 3. Output characteristics

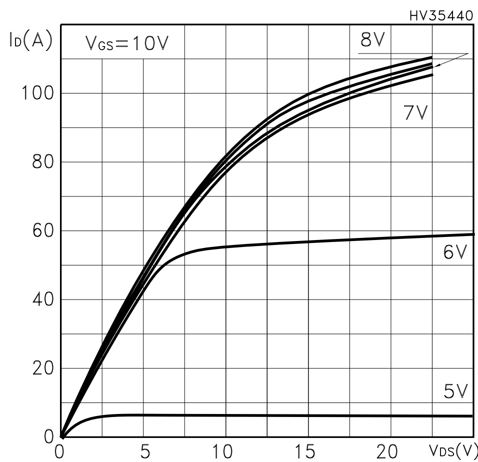


Figure 4. Transfer characteristics

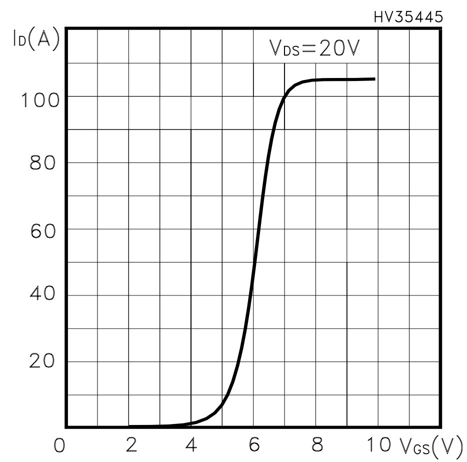


Figure 5. Gate charge vs. gate-source voltage

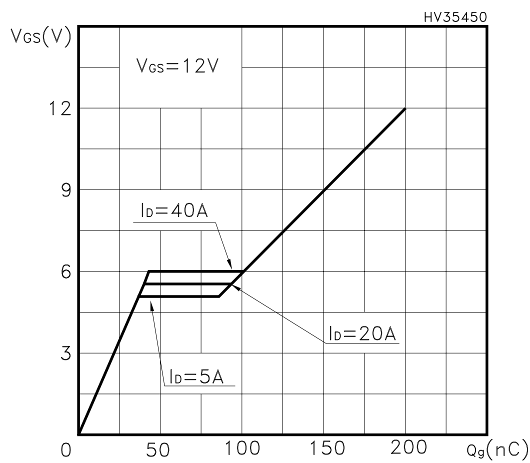


Figure 6. Capacitance variations

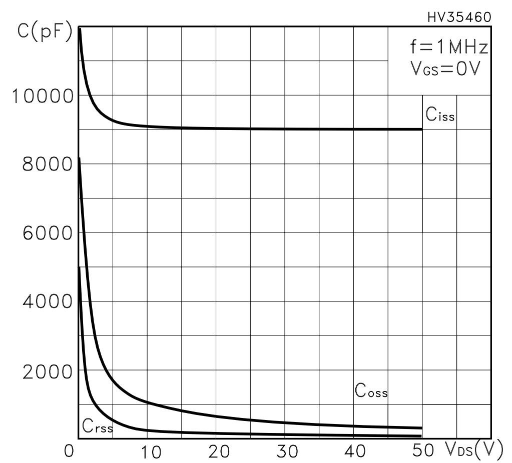


Figure 7. Normalized BV_{DSS} vs. temperature

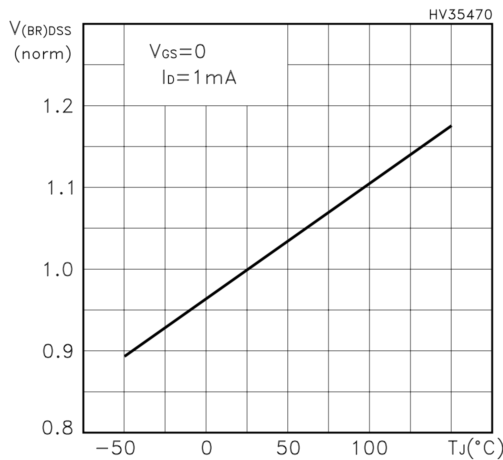


Figure 8. Static drain-source on resistance

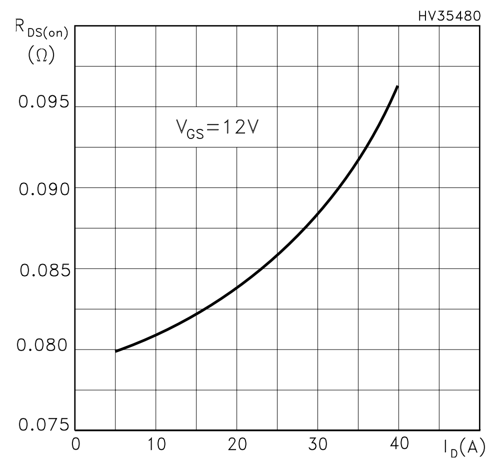


Figure 9. Normalized gate threshold voltage vs. temperature

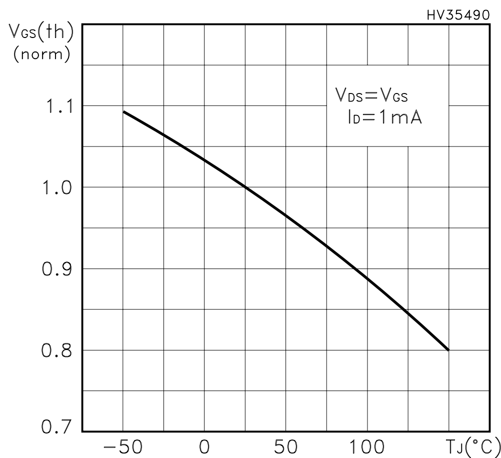


Figure 10. Normalized on resistance vs. temperature

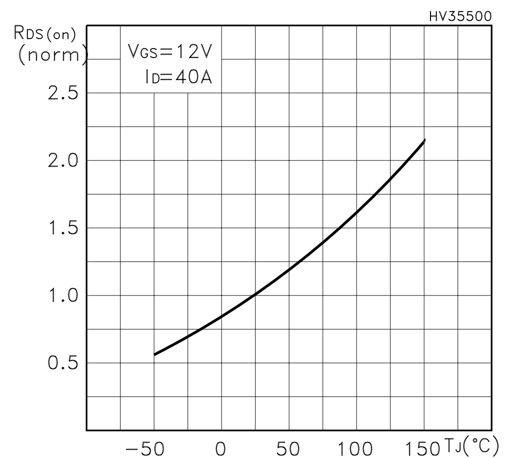


Figure 11. Source drain-diode forward characteristics